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OPTIMIZATION OF CMCU WITH BASE STRUCTURE DEDICATED FOR CPLD SYSTEMS

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Abstract

The method of hardware reduction is proposed which is dedicated for compositional microprogram control unit implemented in CPLD. The method is based on using more than one data source in calculation of microinstruction address. Such approach permits to the decrease the number of logic blocks used for the implementation of the controller in the target CPLD. The paper presents the conditions needed to apply the method. The article contains a calculation example for the presented method.

Keywords: CPLD, PAL, CMCU.

OPTYMALIZACJA CMCU Z BAZOWĄ STRUKTURĄ DEDYKOWANA DLA UKŁADÓW CPLD

Streszczenie

W artykule przedstawiona została metoda zmniejszenia powierzchni sterowników sprzętowych realizowanych w układach typu CPLD. Wprowadzono modyfikacje w strukturze sterownika, modyfikacje których głównym zadaniem jest redukcja liczby wykorzystanych elementów logicznych podczas implementacji sterownika w układach CPLD. Zaprezentowana została bazowa metodologia projektowa, dla której wprowadzono odpowiednie modyfikacje. Modyfikacje, które pozwalają zmniejszyć liczbę potrzebnych elementów logicznych wykorzystanych przy implementacji realizowanego sterownika. Przedstawione modyfikacje bazują na wykorzystaniu więcej niż jednego źródła danych przy wyznaczaniu kolejnego adresu mikroinstrukcji. W artykule przedstawiony został schemat logiczny dla zmodyfikowanej struktury sterownika. Zaprezentowano i omówiono warunki potrzebne do zastosowania zaprezentowanej metody oraz podano odpowiednie przykłady obliczeniowe. W artykule przedstawione zostały wyniki oraz wnioski z badań przeprowadzonych przez autorów.

Słowa kluczowe: CPLD, PAL, CMCU.

1. Introduction

Control units are very important parts of digital systems [2]. Now, complex programmable logic devices (CPLD) are widely used for implementing logic circuits of control units [1, 8]. They include macrocells of programmable array logic (PAL) having the wide fan-in and limited number of terms per macrocell. To optimize the hardware amount in logic circuit of a control unit, the peculiarities of CPLD should be taken into account, as well as features of a control algorithm to be implemented. If a control algorithm is represented by the linear graph-scheme of algorithm (GSA), then the model of compositional microprogram control unit (CMCU) can be used for its interpretation. We assume that CM of CMCU is implemented as PROM memory. In such cases the codes of classes of pseudoequivalent operational linear chains (OLC) [4] can be represented by more than one source due to the wide fan-in of PAL macrocells. In this article we propose some method of CMCU logic circuit optimization based on use of two sources of codes.

2. Conclusion

The proposed method targets on reduction for the number of PAL macrocells in the block of microinstruction addressing (BMA) of CMCU. There are three main factors allowing this reduction:

1. Up-to-day PAL macrocells have the wide fan-in permitting use more than one source for code of OLC.
2. Natural redundancy of PROM chips because their numbers of outputs belong to some limited set. It results in free outputs that can be used for representation of some codes.
3. Existence of the classes of pseudoequivalent OLC allowing decrease for the number of lines of transition table and, therefore, the number of PAL macrocells implementing this table.

Our future research is connected with application of proposed approach for CMCU implementation with FPGAs [5].

3. References

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