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Reduction of the Memory Size in the Microprogrammed Controllers

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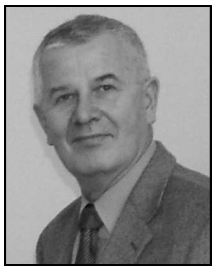

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Abstract

The method of reduction of the control memory size in the microprogrammed controllers is proposed in the article. The idea is based on the hypergraph theory. The concurrent microoperations are encoded together thus the total volume of the memory is reduced. In order to receive the proper microinstruction, an additional module – microinstruction decoder is also prepared. The idea of the proposed method is illustrated by an example. Moreover, the result of performed experimental investigations is presented, as well.

Keywords: hypergraphs, microprogrammed controllers, reduction, memory, microinstruction decoder.

Redukcja pojemności pamięci w sterownikach mikroprogramowanych

Streszczenie

W artykule zaproponowano metodę redukcji pojemności pamięci sterowników mikroprogramowanych. Metoda bazuje na teorii hipergrafów. Mikrooperacje parami kompatybilne są kodowane wspólnie, dzięki czemu redukcji ulega całkowita pojemność pamięci sterownika mikroprogramowanego. Do struktury układu wprowadzono dodatkowy moduł, dekodera mikroinstrukcji. Jednostka ta jest odpowiedzialna za odkodowanie pierwotnych danych. Idea proponowanej metody zilustrowano przykładem. Ponadto, przeprowadzono także badania eksperymentalne, których celem była weryfikacja skuteczności proponowanej metody. Wyniki badań pokazują, że pierwotna pamięć sterownika jest redukowana średnio o 21%.

Słowa kluczowe: hipergrafy, sterowniki mikroprogramowane, redukcja, pamięć, konwerter adresów.

1. Introduction

A control unit (CU) is important part of a digital system [1,2,3,4,5,6]. Usually, the control unit is realized as a finite state machine (FSM) [4,6,7,8]. However, in the case of the linear flowchart, the microprogrammed controller may require less amount of hardware than control unit based on the traditional FSM model [9,10,11]. In case of microprogrammed controllers, the control unit is decomposed into two main parts. The first one addresses microinstructions [7,9], while the second is in response of holding and generating the proper microinstruction [10,12].

Such a solution leads to the reduction of the number of logic elements that are required for implementation of the controller [12]. Typically, the control memory is implemented as a ROM or RAM memory. Thus, wider areas of the destination device can be used for other modules of the prototyped system [1,4,5,7,10,13].

Most of controllers (especially realized as a Complex Instruction Set Computers, CISC) have a long microinstruction width what influences on the memory size [3,5]. Such a situation causes serious problems in the prototyping process. In case of System-On-Programmable-Chip (SoPC), the memory can be implemented with dedicated memory blocks of the Field Programmable Gate Arrays (FPGA). However, if the microinstruction length exceeds the total length of the dedicated memory block of an FPGA, the memory has to be decomposed. On the other hand, in case of controllers implemented as a System-On-Chip (SoC), the memory is designed as an independent module. This means that each additional bit in the microinstruction width increases the total size of the memory and increases the cost of the whole device.

In the paper we propose the method of the control memory reduction. The idea is based on the reduction of the microinstruction length by encoding the concurrent microoperations together. To achieve it, the hypergraph theory is applied [11,14]. Moreover, the particular stages of the reduction process also are performed with hypergraphs. Finally, the initial memory is reduced, while the proper microinstructions are decoded by an additional block of microinstruction decoder.

2. Idea of the proposed method

To reduce the memory size, microinstructions that are pairwise compatible (can be executed concurrently) will be encoded together. Such an idea permits to reduce the total memory size. However, an additional block, Microinstruction Decoder (MD) is also required. Figure 1 illustrates the idea of the proposed method.

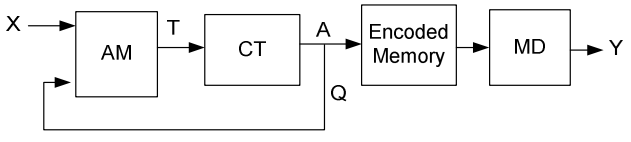

Fig. 1. An idea of the proposed method
Rys. 1. Idea proponowanej metody

The reduction method bases on the hypergraph theory, initially presented in [11,14,15]. The reduction idea was enhanced and adapted to the microprogrammed controllers. The whole process can be divided into the following steps:

1. Formation of the set of compatibility classes.
2. Determination of the weight (cost) of each compatibility class.
3. Calculation of the hypergraph dual to the hypergraph H_C.
4. Determination of the minimum vertex covering (transversal) of hypergraph H_D.
5. Calculation of the total cost of each minimum covering and reduction of redundant microoperations.
6. Encoding compatibility classes which realize minimal transver sal.
7. Determination of a new content of memory with encoded com patibility classes.
8. Formation of the module of Microinstruction Decoder. In the final step the module MD is formed.

Finally, the whole system can be designed. Depending on the designers demands, proper modules can be implemented in various ways [3,4,12,16,17]. For example the addressing module, the counter and the microinstruction decoder may be realized with Look-Up Tables (LUTs), while Encoded Memory can be implemented with dedicated memory blocks of a destination reprogrammable device [5,14].

3. The results of experiments

The effectiveness of the discussed method has been verified experimentally. The library of test modules consists of over 50 benchmarks. All of examined memories were real memory systems of logic controllers and they were taken from specifications and benchmarks presented in [7,9,10,11,12,14,18].

Table 1 shows the results of experiments, where representative benchmarks (memories) are presented.

Tab. 1. Results of experiments
Tab. 1. Wyniki badań eksperymentalnych

Benchmark	Size of the initial memory [bits]	Size of the reduced memory [bits]	Density of the memory	Reduction of the memory [%]
Test022	264	154	19,31%	42%
Test021	176	112	20,45%	36%
TestMK_06	234	162	28,63%	31%
TestMK_10	180	135	27,22%	25%
Test016	25	20	28,00%	20%
Test032	168	140	41,66%	17%
Test012	60	55	71,66%	8%
Average	**72,93**	**57,58**	**35,66%**	**21%**

From above tables we can see that application of the proposed method permits to reduce the volume of the memory on average by 21%. All of the examined memories were reduced (the lowest reduction was equal to 8%, while the highest – 42%). It means, that the size of reduced memory in microprogrammed controllers is always smaller than the initial one.

It is worth to notice, that effectiveness of the reduction process strongly depends on the density of the initial memory. Results of experiments have shown that reduction is especially high in case of density lower than 30% of the initial memory. For example the memory of Test022 can be reduced over than 40%. On the other hand, there are controllers which memories are hard to reduce with higher density, and the reduction may be less than 10%.

4. Conclusions

The method of reduction of microprogrammed controllers memory was presented in the paper. The idea was based on the hypergraph theory. An initial memory is represented by a hypergraph. Further computations lead to the reduced memory, where microoperations are encoded. The results of experiments have shown, that effectiveness of the proposed method strongly depends on the density of the initial memory.

5. References

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