Logic Controllers Design Towards Partial Reconfiguration

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***Abstract*—The paper presents method for hierarchical configurable Petri nets description in VHDL language. Dual model is an alternative way for behavioral description of the discrete control process. Dual model consists of two correlated models: UML state machine diagram and hierarchical configurable Petri net (HCfgPN). HCfgPN are Petri nets variant with direct support of exceptions handling mechanism. Logical synthesis of dual model is realized by the description of HCfgPN model by means of hardware description language. The paper presents places-oriented method for HCfgPN description in VHDL language.**

***Index Terms*—HCfgPN, UML state machine diagram, VHDL, logic controller**

I. Introduction

Device implementation of reconfigurable logic controllers (RLCs) with the use of Field Programmable Gate Array devices (FPGA) is a quite commonly used solution. Modern Integrated Circuits (ICs), including FPGA devices, provide opportunity for implement faster, bigger and betters solutions. Improved techniques for design should follow the growing technological capabilities, allowing for full use. Dynamic Partial Reconfiguration is a good example of powerful functionality.

The paper presents modular approach for Logic Controllers (LCs) developing based on UML state machines and Petri nets. Full and coherent modularity on each stage of developing process simplifies and streamlines the design of LCs oriented for partial reconfiguration [1], [2]. The application of Partial Reconfiguration in the field of LCs, improve its quality not only by improving the functionality but also by reducing power consumption and minimization of allocated resources. The application of the modern specification technics, UML language in particular [3], will simplify partial reconfiguration oriented design. Petri nets give the possibility for logic controller formal verification.

II. Partial reconfiguration

Classical design flow of LCs with final with the finale in the form of implementation in FPGA consider preparation of one final `.bit` or `.mcs` file. In this approach full static reconfiguration requires reload of whole FPGA device configuration which cause interrupt control. In the Difference based partial reconfiguration (DBPR) oriented developing process, two configurations are compared and, as a result, differential configuration file is generated. This approach is dedicated rather for small design changes e.g. Block Ram contents modification [4].

Full benefits from the partial-oriented design comes with modular based partial reconfiguration (MBPR). In the design static modules (SMs) and reconfigurable partitions (RPs) are identified. For each RP, set of alternative reconfigurable modules (RMs) is developed. The bottom-up synthesis is performed and each module is synthesized separately, finally top-level module unite both static and reconfigurable modules. During dynamic module-based partial reconfiguration, structure of separated reconfigurable partition may be changed without affecting the operation of other modules

III. LCs design towards Partial reconfiguration

UML state machine and Hierarchical Configurable Petri Net are two component models of the Dual Specification [5]. Modularity of the DS, simplify functional decomposition of the control system. Each composite state or macroplace is responsible for particular functionality implementation. Each functional block is implemented as separated module and may be reconfigured independent.

Also new techniques must be developed to ensure the determinism of the control algorithm realization during the partial reconfiguration. Although it is a dynamic reconfiguration, the unwanted effects may occur in the execution flow of the control algorithm, when the reconfigured module will be active and involved in the control algorithm realization. Modern FPGA devices requires refreshing new approach for partial reconfigurable logic controllers developing. Its also caused by technological changes e.g. no bus macros between modules is required [6]. The paper presents full path of the partial-reconfigurable oriented logic controller developing process. Actual PR-flow for modular design and reconfiguration was applied for UML state machines and Petri nets specification.

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