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Optimization of logic circuit of Moore FSM on CPLD

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Abstract

Method of decrease of number of PAL macrocells in the circuit of Moore FSM is proposed. Method is based on usage of free outputs of embedded memory blocks to represent the code of the class of the pseudoequivalent states. Proposed approach permits to decrease the hardware amount without decrease of digital system performance. An example of application of proposed method is given.

Keywords: Moore finite-state-machine, PAL macrocells, CPLD, embedded memory blocks, flow-chart of algorithm.

Optymalizacja skończonych automatów Moore'a w układach CPLD

Streszczenie

W pracy przedstawiona została metoda zmniejszania ilości makro-komórek w układach typu PAL przy pomocy automatów Moore'a FSM. Metoda ta jest oparta na wykorzystaniu nieużywanych wyjść osadzonych obszarów pamięci w celu reprezentacji kodu klasy pseudo-równoważnych stanów. Zaproponowane podejście pozwala zmniejszyć ilość wymaganego zużycia sprzętowego bez zmniejszenia wydajności systemów cyfrowych. Podany również jest przykład aplikacji zaproponowanego rozwiązania.

Słowa kluczowe: automat Moore'a, PAL makro-komórka, CPLD, wbudowany blok pamięci, schemat blokowy algorytmu.

1. Introduction

A control unit is very important block of any digital system, its function is coordination of other blocks interplay [1, 7]. A model of Moore finite-state-machine (FSM) is used very often to represent the control unit [5, 6]. The current state of microelectronics permits to implement a complex digital system using single chip of the "system-on-a-chip" (SoC) type [11, 12]. An arbitrary logic of a digital system can be implemented using PAL (programmable array logic) macrocells of SoC, if they used CPLD (complex programmable logic devices) approach [8]. The tabular functions can be implemented using embedded memory blocks of the SoC [5]. One of actual problems is decrease of the hardware amount in the logic circuit of control unit [6]. The solution of this problem permits to decrease the chip area occupied by circuit of control unit and it gives the potential possibility to increase the amount of digital system functions inside single chip. The peculiarities of both PAL macrocells and model of control unit should be taking into account to solve this problem [5]. The peculiarities of PAL are wide fan-in of macrocells and very limited number of terms per macrocell [10, 12]. The peculiarities of Moore FSM are existence of pseudoequivalent states and regular character of system of microoperations that permits its implementation using embedded memory blocks [2, 3]. In this article we propose the method of optimization of the amount of PAL macrocells in the logic circuit of Moore FSM using the above mentioned peculiarities.

2. Background of Moore FSM design

Let control algorithm of digital system is specified by flow-chart of algorithm (FCA) [6] $\Gamma = \Gamma (B, E)$, where $B = \{b_0, b_E\} \cup E_1 \cup E_2$ is set of the vertices and E is set of the edges. Here b_0 is initial vertex, b_E is final vertex, E_1 is set of operational vertices, E_2 is set of conditional vertices. The vertex $b_q \in E_1$ contains a collection of microoperations $Y(b_q) \subseteq Y$, where $Y = \{y_1, ..., y_N\}$ is set of microoperations of data-path [7] of digital system. The vertex $b_q \in E_2$ contains a logic condition $x_e \in X$, where $X = \{x_1, ..., x_L\}$ is set of logic conditions (flags) [1]. The initial and final vertices of FCA correspond to initial state $a_1 \in A$, where $A = \{a_1, ..., a_M\}$ is set of internal states of Moore FSM. Each operational vertex $b_q \in E_1$ corresponds to unique state $a_m \in A$ and collection $Y(b_q) = Y(a_m)$. The logic circuit of Moore FSM U_1 set up by systems of Boolean functions:

$$\Phi = \Phi (T, X), \tag{1}$$

$$Y = Y (T), \tag{2}$$

where $T = \{T_1, ..., T_R\}$ is set of internal variables to encode the states $a_m \in A$, $R =]\log_2 M[$; $\Phi = \{D_1, ..., D_R\}$ is set of excitation functions of the FSM memory.

The structural diagram of Moore FSM U_1 is shown in Fig. 1.

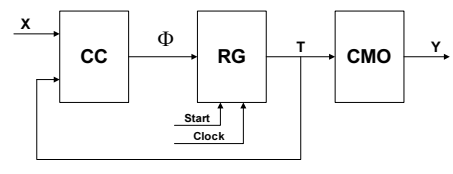

Fig. 1. Structural diagram of Moore FSM U_1
Rys. 1. Struktura diagramu Moore'a FSM U_1

Here combinational circuit CC forms functions (1), which are the excitation functions of D flip-flops of register RG. Circuit CMO forms microoperations (2). The pulse Start is used to load the code of initial state into RG, pulse Clock is used to change the

content of RG from code $K(a_m)$ of current state $a_m \in A$ to code $K(a_S)$ of the next state $a_S \in A$. In case of CPLD-based SoC circuit CC is implemented using PAL macrocells and circuit CMO is implemented using embedded memory blocks [12].

The base to form the systems (1)-(2) is the direct structural table (DST) [7] with columns: a_m is current state of FSM; $K(a_m)$ is code of current state having R bits; a_S is state of transition, $K(a_S)$ is code of this state, X_h is conjunction of some elements of the state X (or their complements), that causes transition $<a_m, a_S>$; $\Phi_h \subseteq \Phi$ is collection of excitation functions that are equal to 1 to switch RG from $K(a_m)$ into $K(a_S)$; h is a number of transition ($h = 1, \ldots, H_1(\Gamma)$). The column a_m contains the collection $Y(a_m) \subseteq Y$.

As a rule, the number of transitions $H_1(\Gamma)$ exceeds the number of transitions $H_2(\Gamma)$ of equivalent Mealy FSM [2]. It leads to increase of the amount of PAL macrocells (hardware amount) and sometimes number of levels in the circuit CC of Moore FSM in comparison with these characteristics of equivalent Mealy FSM [5]. The value $H_1(\Gamma)$ can be decreased by taking into account the existence of pseudoequivalent states of Moore FSM [1]. The states a_m, $a_S \in A$ are pseudoequivalent states, if the outputs of corresponding operational vertices are connected with the input of the same vertex of FCA Γ. Let $\Pi_A = \{B_1, \ldots, B_I\}$ is partition of the set A by the classes of pseudoequivalent states ($I \le M$). Let us encode the class $B_i \in \Pi_A$ by binary code $K(B_i)$ with $R_1 =]\log_2 I[$ bits. Let us use the variables $\tau_r \in \tau$ for such encoding, where $|\tau| = R_1$.

In this case special code transformer TC can be introduced into circuit of U_1. It forms the codes $K(B_i)$ on the base of the codes $K(a_m)$, where $a_m \in B_i$. Now circuit CC forms functions

$$\Phi = \Phi (\tau, X), \tag{3}$$

and circuit TC forms functions

$$\tau = \tau (T). \tag{4}$$

The circuit TC is implemented using embedded memory blocks of SoC [5].

It is proved, that system (3) has $H_2(\Gamma)$ terms [2]. But such approach has one drawback: it consumes additional resource of embedded memory blocks to implement the circuit of TC.

In this work we propose the design method that permits to decrease the hardware amount in the circuit CC without code transformer. The proposed method is based on the following peculiarities of CPDL [8, 10, 12]:

- the fan-in of PAL macrocells exceeds significantly the maximal possible number of literals in the terms of the system (1), that is equal to $L+R$;
- the number of outputs of embedded memory block can be chosen from some restricted area {1, 2, 4, 8 }.

3. Main idea of proposed method

Let t_F is fixed number of outputs of the embedded memory block and let q is amount of its words, if $t_F = 1$. The value t_F for FSM U_1 is determined as

$$t_F =] q / M [. \tag{5}$$

The total amount of the outputs t_S of all embedded memory blocks in the circuit CMO is determined as

$$t_S =] N / t_F [* t_F. \tag{6}$$

In this case

$$\Delta_t = t_S - N \tag{7}$$

outputs are not in use to represent the microoperations $y_n \in Y$.

Let us represent the set Π_A as $\Pi_A = \Pi_B \cup \Pi_C$, where $B_i \in \Pi_B$, if condition

$$|B_i| > 1 \tag{8}$$

holds, and $B_i \in \Pi_C$, if condition (8) is violated. It is clear that block TC should forms only the codes of the classes $B_i \in \Pi_B$. Let us encode each class $B_i \in \Pi_B$ by binary code $K(B_i)$ with

$$R_2 =]\log_2 (M_1 + 1)[\tag{9}$$

bits, where $|M_1| = \Pi_B$ and "1" is added to indicate the case, when $B_i \notin \Pi_B$. Let us use the variables $z_r \in Z$ for such encoding, where $|Z| = R_2$. Let us discuss the case, when condition

$$\Delta_t \ge R_2 \tag{10}$$

holds. In this case FCA Γ can be interpreted by proposed Moore FSM U_2 (Fig. 2).

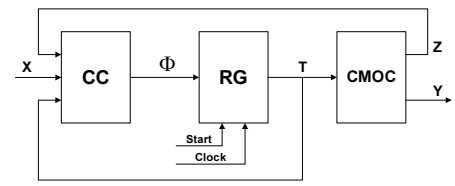

Fig. 2. Structural diagram of Moore FSM U_2
Rys. 2. Struktura diagramu Moore'a FSM U_2

Here circuit CC forms functions

$$\Phi = \Phi (T, Z, X), \tag{11}$$

circuit CMOC forms functions (2) and functions

$$Z = Z (T). \tag{12}$$

The variables $T_r \in T$ represent the codes $K(a_m)$, where $a_m \in B_i$ and $B_i \in \Pi_C$. Such approach permits to decrease the number of terms in the system Φ up to $H_2(\Gamma)$ and number of embedded memory blocks are equal for both CMO and CMOC. As we can see, circuit U_2 does not include TC. The number of inputs in the PAL macrocells of U_2 is increased up to $L+R+R_2$, but it does not affect the hardware amount in the circuit CC in comparison with Moore FSM with TC. The cycle time of both U_1 and U_2 is the same in the worst case. In the best case, if circuit CC of U_2 has less levels, than circuit CC of U_1, the time of cycle of U_2 is less, that time of cycle of U_1. Therefore, the proposed approach permits to decrease hardware amount without decrease of digital system performance.

The method of design of logic circuit of U_2 differs from design method of U_1 [6] only in some details. They are connected with estimations of values (7), (9), (10) and construction of modified DST (MDST) to form the functions (11). Let us discuss an example of design of Moore FSM $U_2(\Gamma_1)$, where symbol $U_i(\Gamma_j)$ stays for interpretation of FCA Γ_j by Moore FSM with structure U_i.

4. Example of proposed method application

Let control algorithm of a digital system is represented by marked FCA Γ_1, where $M = 16$. Let FCA Γ_1 is set up by system of formulae of transitions [6], where vertices $b_q \in E_2$ are replaced by corresponding states $a_m \in A$:

$$\begin{aligned}
&a_1 \rightarrow a_2;\ a_2 \rightarrow a_3;\ a_7 \rightarrow a_8;\ a_{15} \rightarrow a_{16};\ a_{16} \rightarrow a_1;\\
&a_3 \rightarrow x_1x_2a_4 \vee x_1/x_2a_5 \vee /x_1x_3a_6 \vee /x_1/x_3a_7;\\
&a_4, a_5, a_6 \rightarrow x_3x_4a_8 \vee x_3/x_4a_9 \vee /x_3x_5a_{10} \vee /x_3/x_5a_7;\\
&a_8, a_9, a_{10} \rightarrow x_4x_3a_{11} \vee x_4/x_3a_{12} \vee /x_4x_5a_{13} \vee /x_4/x_5a_{14};\\
&a_{11}, a_{12}, a_{13}, a_{14} \rightarrow a_{15}.
\end{aligned} \tag{13}$$

It is follows from (13) that $M = 16$, $R = |T| = |\Phi| = 4$, $\Pi_A = \{B_1, \ldots, B_9\}$, where $B_1 = \{a_1\}$, $B_2 = \{a_2\}$, $B_3 = \{a_3\}$, $B_4 = \{a_4, a_5, a_6\}$, $B_5 = \{a_7\}$, $B_6 = \{a_8, a_9, a_{10}\}$, $B_7 = \{a_{11}, a_{12}, a_{13}, a_{14}\}$, $B_8 = \{a_{15}\}$, $B_9 = \{a_{16}\}$. Let N = 14, $t_F = 4$, it means $q = 64$. An analysis of Π_A gives us $\Pi_B = \{B_4, B_6, B_7\}$ and $\Pi_C = \{B_1, B_2, B_3, B_5, B_8, B_9\}$.

Therefore, $M_1 = 3$, $R_2 = |Z| = 2$ as it follows from (9). The condition (10) holds and application of proposed method has sense.

Let microoperations $y_n \in Y$ are distributed among the states of FSM in the following order: $Y(a_1) = \emptyset$, $Y(a_2) = Y(a_6) = \{y_1, y_3\}$, $Y(a_3) = Y(a_{16}) = \{y_2, y_4, y_6\}$, $Y(a_4) = Y(a_8) = Y(a_{12}) = \{y_1, y_7, y_8\}$, $Y(a_5) = \{y_3, y_5, y_9\}$, $Y(a_7) = \{y_{10}, y_{11}\}$, $Y(a_9) = \{y_{12}, y_{12}\}$, $Y(a_{10}) = \{y_1, y_{13}, y_{14}\}$, $Y(a_{11}) = Y(a_{15}) = \{y_4, y_{13}\}$, $Y(a_{13}) = \{y_7, y_9\}$, $Y(a_{14}) = \{y_2, y_{12}\}$. Let us encode the classes $B_i \in \Pi_B$ in the following manner: $K(B_4) = 01$, $K(B_6) = 10$, $K(B_7) = 11$. The code <00> corresponds to all blocks $B_i \in \Pi_C$. Let states of FSM are encoded in a trivial way: $K(a_1) = 0000$, …, $K(a_{16}) = 1111$. Let code $K(B_i)$, where $B_i \in \Pi_C$, is equal to code $K(a_m)$, where $a_m \in B_i$.

To form the MDST of Moore FSM U_2 the states $a_m \in B_i$ should be replaced by classes $B_i \in \Pi_A$ in the left parts of all formulae of transitions. Such transformation of the system (13) leads to system (14):

$$B_1 \rightarrow a_2;\ B_2 \rightarrow a_3;\ B_3 \rightarrow x_1x_2a_4 \vee x_1/x_2a_5 \vee /x_1x_3a_6 \vee /x_1/x_3a_7;$$
$$B_4 \rightarrow x_3x_4a_8 \vee x_3/x_4a_9 \vee /x_3x_5a_{10} \vee /x_3/x_5a_7;$$
$$B_5 \rightarrow a_8;\ B_6 \rightarrow x_4x_3a_{11} \vee x_4/x_3a_{12} \vee /x_4x_5a_{13} \vee /x_4/x_5a_{14};$$
$$B_7 \rightarrow a_{15};\ B_8 \rightarrow a_{16};\ B_9 \rightarrow a_1. \qquad (14)$$

The MDST includes the columns: B_i, $K(B_i)$, $K(a_m)$, a_S, $K(a_S)$, X_h, Φ_h, h. In case of Moore FSM $U_2(\Gamma_1)$ this table has $U_2(\Gamma_1) = 18$ lines. The first 6 lines of MDST are shown in Table 1.

Tab. 1. Fragment of MDST of Moore FSM $U_2(\Gamma_1)$
Tab. 1. Fragment tabeli MDST Moore'a FSM $U_2(\Gamma_1)$

B_i	$K(B_i)$	$K(a_m)$	a_S	$K(a_S)$	X_h	Φ_h	h
B_1	00	0000	a_2	0001	1	D_4	1
B_2	00	0001	a_3	0010	1	D_3	2
B_3	01	-	a_4	0011	x_1x_2	D_3D_4	3
			a_5	0100	x_1/x_2	D_2	4
			a_6	0101	$/x_1x_3$	D_2D_4	5
			a_7	0110	$/x_1/x_3$	D_2D_3	6

This table is the base to form the system (11). For example, from Table 1 we can get the part of disjuntional normal form of excitation function D_3, where

$$D_3 = /z_1\,/z_2\,/T_1\,/T_2\,/T_3\,T_4 \cup /z_1\,z_2\,x_1\,x_2 \cup /z_1\,z_2\,/x_1\,/x_3.$$

The PAL implementation of the function D_3 is shown in Fig. 3.

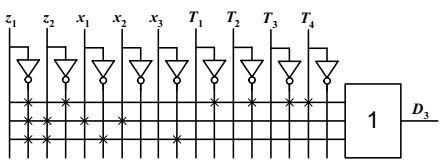

Fig. 3. Implementation of function D_3
Rys. 3. Implementacja funkcji D_3

The table of CMOC includes the columns a_m, $K(a_m)$, $Y(a_m)$, $K(B_i)$, m. It is formed in a trivial way and in case of FSM $U_2(\Gamma_1)$ it has $M = 16$ lines. The first 8 lines are shown in the Table 2.

Tab. 2. Fragment of table of CMOC of Moore FSM $U_2(\Gamma_1)$
Tab. 2. Fragment tabeli CMOC Moore'a FSM $U_2(\Gamma_1)$

a_S	$K(a_m)$	$Y(a_m)$	$K(B_i)$	m
a_1	0000	-	00	1
a_2	0001	y_1y_3	00	2
a_3	0010	$y_2y_4y_6$	00	3
a_4	0011	$y_1y_7y_8$	01	4
a_5	0100	$y_3y_5y_9$	01	5
a_6	0101	y_1y_3	01	6
a_7	0110	$y_{10}y_{11}$	00	7
a_8	0111	$y_1y_7y_8$	10	8

In case of $U_2(\Gamma_1)$ this table has $N + R_2 = 16$ outputs, each output corresponds to single bit of the output word of embedded memory block. The code $K(a_m)$ is treated as an address of embedded memory block word with one-hot codes of microoperations [3] and maximal codes of the classes $B_i \in \Pi_A$. To implement the systems (2) and (12) it is enough

$$\eta_M =]\ N / t_F\ [\qquad (15)$$

blocks embedded memory block with $q \geq M$. In case of $U_2(\Gamma_1)$ we have $\eta_M = 3$.

The implementation of logic circuit of Moore FSM U_2 is reduced to implementation of system (11) using PAL macrocells and implementation of systems (2) and (12) using embedded memory blocks. There are effective methods of these tasks' solution [10,12], but they are out the scope of our article.

5. Conclusion

Experiments were performed using probability based method, which is presented in [4]. Because the actual experiment is quite complicated, it is beyond the scope of this article. The proposed method permits to decrease the amount of PAL macrocells in the circuit that forms excitation functions of FSM memory. The researches of the authors show that this decrease is proportional to coefficient

$$\eta = H_1(\Gamma) / H_2(\Gamma). \qquad (16)$$

Let us point out that value $H_2(\Gamma)$ is equal to the number of transitions of equivalent Mealy FSM. The application of proposed method is possible only, if condition (10) holds. Our researches shown that in this case the hardware amount in the circuit of FSM $U_2(\Gamma)$ can be up to 26-28% less, than in circuit of FSM $U_1(\Gamma)$. The main direction of the future research is comparison the proposed methods with known methods from [9, 10, 12, 13].

6. References

[1] Adamski M., Barkalov A. Architectural and Sequential Synthesis of Digital Devices. - Zielona Gora: University of Zielona Gora Press, 2006, 199 s.
[2] Barkalov A. A. Principles of optimization of logical circuit of Moore finite-state machine. //Cybernetics and system analysis. - 1998, №1, pp. 65-72.
[3] Barkalov A. A. Synthesis of Control Units on PLDs – Donetsk, DonNTU, 2002 (in Russian), 262 pp.
[4] Barkalov A. A. and Barkalov A. Design of Mealy Finite State Machines with transformation of Object Codes. International Journal of Applied Mathematics and Computer Science, Vol.15, No.1, pp.151-158.
[5] Barkalov A., Wegrzyn M. Design of Control Units with Programmable Logic. - Zielona Gora: University of Zielona Gora Press, 2006, 150 s.
[6] Baranov S. Logic Synthesis for Control Automata. - Kluwer Academic Publishers, 1994, 232 pp.
[7] De Micheli G. Synthesis and Optimization of Digital Circuits. McGraw Hill: NY, 1994, 541 pp.
[8] Grushnitsky R., Mursaev A., Ugrjumov E. Development of systems on chips with programmable logic. - SPb: BHV - Petersburg, 2002 (in Russian), 608 pp.
[9] Kania D. Efficient approach to synthesis of multioutput Boolean functions on PAL-base devices. – IEE Proc Comp. Digit. Techn., Vol. 150, No. 3, pp.143-149.
[10] Kania D. Synteza logiczna przeznaczona dla matrycowych struktur programowalnych typu PAL. - Zeszyty naukowe Politechniki Śląskiej, Gliwice, 2004, 240 s.
[11] Maxfield C. The Design Warrior's Guide to FPGA. - Elsevier, NJ, 2004, 542 pp.
[12] Solovjev V. Design of digital systems using the programmable logic integrate circuits. - Moscow: Hot line - Telecom, 2001 (in Russian), 636 pp.
[13] Klimowicz A., Sołowjew W. Wykorzystanie wyjściowych makrokomórek układu PLD w charakterze elementów pamięci automatu skończonego. RUC, Szczecin: Politechnika Szczecińska, 2002.

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